24.3 A 14mW 6.25Gb/s Transceiver in 90nm CMOS for Serial Chip-to-Chip Communications

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Present-day computing systems require very high off-chip communications bandwidth, and multi-Gb/s serial links for chip-to-chip interconnect are now ubiquitous. As system designers face hard power limits due to thermal or battery-life requirements, optimizing power versus performance becomes more critical. Backplane transceivers have been demonstrated at about 20mW/Gb/s [1], and chip-to-chip links have more recently achieved power efficiencies near 10mW/Gb/s [2]. A further significant advance in power efficiency for these links is possible without sacrificing the jitter performance or signal integrity features required to operate at an acceptable BER.

This paper presents a 6.25Gb/s NRZ transceiver in 90nm dual-gate (1.0V, 2.5V) CMOS designed to satisfy modest channel requirements with mesochronous timing. The transceiver dissipates 2.2mW/Gb/s, a 3.4× improvement of the power efficiency reported in [3]. The test chip includes 4 transceivers with shared LC-PLL, a support block with 4 PRBS generator/checkers, and an interface to an external controller. Power reduction is achieved using a shared LC-PLL for reference-clock multiplication, a resonant clock-distribution network, a low-swing voltage-mode transmitter, a low-power phase rotator for the receiver clocks, and software-based CDR and adaptive equalization.

Figure 24.3.1 shows the clock multiplication and distribution scheme. A 195MHz reference clock is multiplied to half the bit rate in a fairly conventional CMOS LC-PLL with 4MHz loop bandwidth. Frequency is coarsely trimmed by switching in metal-metal capacitors as in [4], and phase locked using NMOS accumulation-mode varactors. A conventional divider, phase-frequency detector, charge pump, and loop filter complete the PLL. The oscillator output is buffered to give 600mV swing on the clock distribution network, which is tuned for resonance with Q equal to 3 by placing an inductor across the complementary clock wires at each end. Without the inductors, the inverter-based buffer would consume 3× the power to produce the low-swing clock, and 5× the power to produce a full swing clock. An on-chip ADC allows the controller to measure the varactor bias, oscillator output voltages, and clock distribution voltages. This enables the controller to set the frequency trim and adjust the swing and common-mode voltages of the oscillator and distributed clock to optimize power across process variation.

Figure 24.3.2 is a block diagram of the transmitter. The output stage is an N-over-N low-swing voltage-mode differential driver, much like the one used in [3]. The output swing is set by a locally regulated power supply *Vs*, adjustable to provide an output signal swing of 50 to 300mV$_{pp\text{-}diff}$. A large internal bypass capacitor on the *Vs* supply completes the differential termination path. The return impedance of the transmitter is set by a second internally regulated supply voltage *Vr* that sets the signal swing of the predriver. It is generated by forcing the impedance of a replica transmitter to match the resistance of a resistor R, a multiple of the line impedance. The CMOS 2:1 MUX is driven by a buffered copy of the distributed reference clock; buffer fanout is small to hold DJ as low as possible. The 16:2 MUX is a tree of 2:1 MUX stages, clocked by a divider chain.

Figure 24.3.3 is a block diagram of the receiver. The line input is amplified by 6dB and level shifted in an NMOS common-gate amplifier. A source-degenerated EQ amplifier provides up to 8.5dB of peaking at 3.125GHz, adjustable under software control. Offset from the 2 amplifier stages is removed at the output of the common-gate amplifier. The EQ amplifier drives a bank of 4 offset-trimmed samplers that form an Alexander phase detector for clock/data recovery. Both edge and data samples are deserialized in identical 2:16 trees of DEMUX elements. The edge samplers and deserializer are enabled infrequently by the controller to implement a low-bandwidth CDR. A PLL-based phase rotator sets the phase of the sampler clocks by introducing a phase shift relative to the reference clock, with 62 steps per UI. The controller programs the phase rotator and EQ amplifier based on an analysis of the deserialized data and edge samples.

Figure 24.3.4 is a block diagram of the receiver phase-rotator PLL, similar to the one described in [5]. A 4-stage CMOS oscillator generates the quadrature sampling clocks. The oscillator is powered from the regulated supply *Vosc*, which is controlled by a 2-stage regulator. The top (series) regulator, a heavily bypassed current source, provides power-supply isolation and is driven by a slow control loop implemented in software. The lower (shunt) regulator provides phase and frequency lock. With the frequency detector enabled, the controller adjusts *icoarse* so that the PLL loop control voltage *Vctl* is near a target voltage; it then hands control from the frequency detector to the fine phase-control loop. An XOR-style phase mixer/detector introduces a programmable phase shift in the feedback path of the PLL. The PLL shunt regulator can be sized to reduce loop gain, allowing the loop filter to be implemented with small capacitors.

The test chip is packaged in a wire-bonded BGA, and mounted onto a test board using a pogo-pin socket. Transceivers are connected to edge-launch SMAs through 9.5cm of FR4 microstrip.

The upper portion of Fig. 24.3.5 shows the phase-noise of a transmitter sending a 6.25Gb/s (1010...) pattern, integrating to RJ of 1.27ps$_{rms}$ over a bandwidth from 100Hz to 1GHz. The lower portion shows an eye diagram of the transmitter sending a 2^{23}-1 PRBS sequence measured at the board edge; the nominal output swing is 200mV$_{ppd\text{-}diff}$, and DJ is 20ps$_{pp}$, primarily due to fixturing.

Link experiments are run with various interconnects inserted between 2 test chips. The upper portion of Fig. 24.3.6 shows the frequency response of the demonstration channel, with attenuation of -15dB at 3.125GHz. The lower portion shows the BER versus receiver phase offset for transmitter swings of 210 and 130mV$_{pp\text{-}diff}$. The plots yield estimated BERs of 10^{-30} and 10^{-23} respectively, and demonstrate a voltage margin of >70mV$_{pp\text{-}diff}$. The link was run for 2 days with no errors at 130mV$_{pp\text{-}diff}$, indicating that at nominal swing it operates with margin at a BER $<10^{-15}$.

The measured power consumption per transceiver is 13.8mW under nominal conditions. A transmitter consumes 4.9mW, a receiver consumes 8.0mW, and the shared LC-PLL and clock distribution network together consume 3.6mW (0.9mW per transceiver). A single transceiver occupies 0.307mm^2, 25% of which is V_{DD} bypass capacitor implemented in 2.5V thickox. The LC-PLL is 0.228mm^2, of which 6% is V_{DD} bypass capacitor. Area calculations include wirebond pads. The design uses standard-V_t 1V devices, 2.5V thickox standard and native devices, and the NMOS accumulation-mode varactor.

References:

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[3] K.-L. J. Wong, H. Hatamkhani, M. Mansuri, et al., "A 27-mW 3.6-Gb/s I/O Transceiver," *IEEE J. Solid-State Circuits*, vol. 39, pp. 602-612, Apr., 2004.

[4] H. Sjöland, "Improved Switched Tuning of Differential CMOS VCOs," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, pp. 352-355, May, 2002.

[5] T. Toifl, C. Menolfi, P. Buchmann, et al., "0.94ps-rms-Jitter 0.016mm^2 2.5GHz Multi-Phase Generator PLL with 360° Digitally Programmable Phase Shift for 10Gb/s Serial Links," *ISSCC Dig. Tech. Papers*, vol. 48, pp 410-411, Feb., 2005.

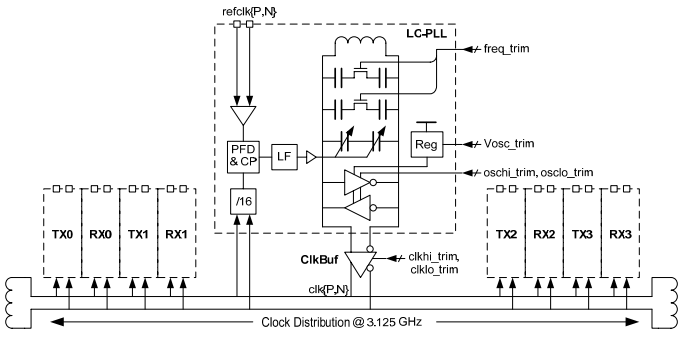


Figure 24.3.1: Clock multiplication and distribution.

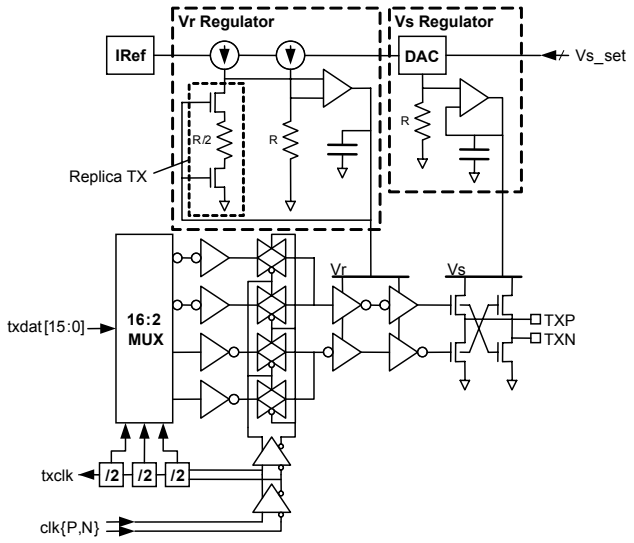


Figure 24.3.2: Transmitter block diagram.

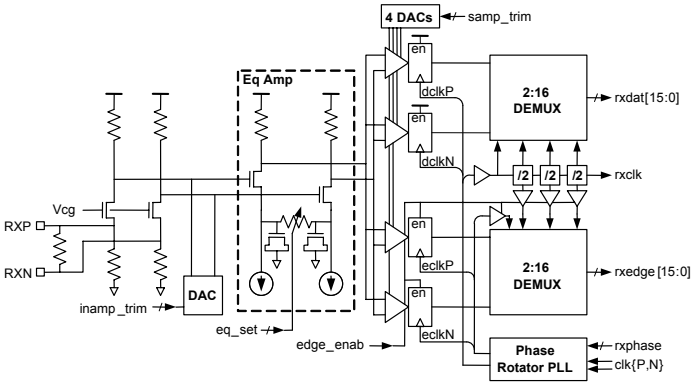


Figure 24.3.3: Receiver block diagram.

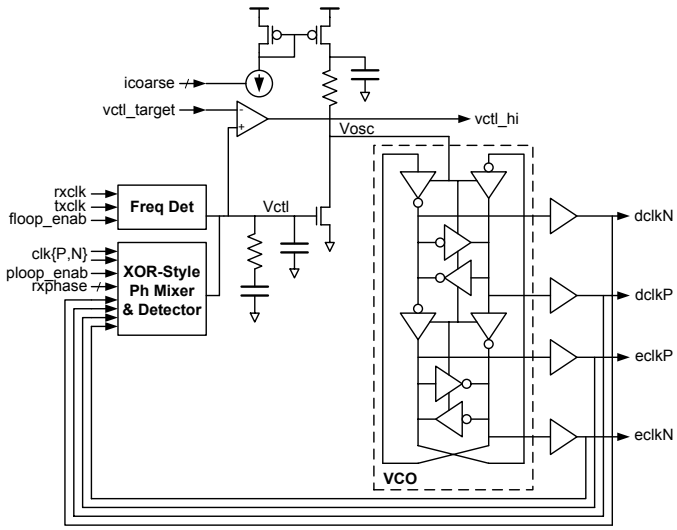
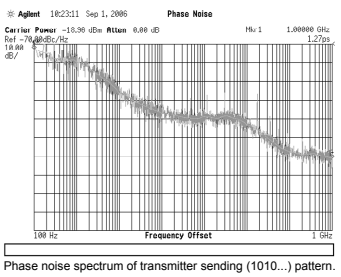
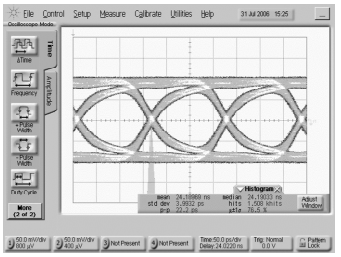


Figure 24.3.4: Phase-rotator PLL block diagram.

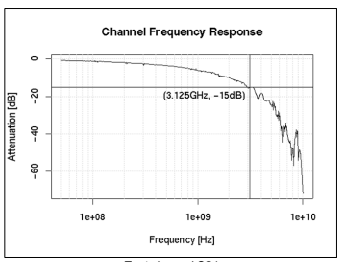


Phase noise spectrum of transmitter sending (1010...) pattern.

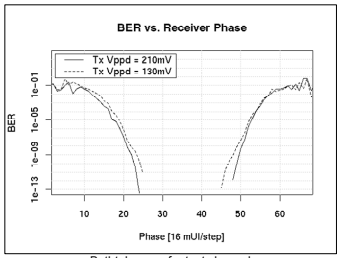


6.25Gb/s transmitter eye of PRBS sequence at test board edge.

Figure 24.3.5: Transmitter output jitter.



Test channel S21.



Bathtub curve for test channel.

Figure 24.3.6: Link measurements.

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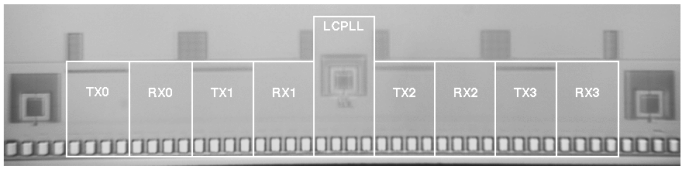

Figure 24.3.7: Die micrograph.

